



Ministry of Higher Education and
Scientific Research - Iraq

University of Warith Al Anbiyaa
Engineering College
Biomedical Engineering Department



Module Information

Module Title	Digital Electronics			Module Delivery	
Module Type	Core			☒Theory ☒Lecture ☒Lab ☐Tutorial ☐Practical ☐Seminar	
Module Code	BME-322				
ECTS Credits	6				
SWL (hr/sem)	175				
Module Level		3	Semester of Delivery		2
Administering Department		BME	College	ENG	
Module Leader	Asst. Lec. Ali Mohammed		e-mail	Ali.mohammed@uowa.edu.iq	
Module Leader’s Acad. Title		Asst.Lec	Module Leader’s Qualification		Mse
Module Tutor			e-mail	E-mail	
Peer Reviewer Name		Name	e-mail	E-mail	
Scientific Committee Approval Date		09/02/2026	Version Number		1.0

Relation with other Modules			
Prerequisite module	Electronics	Semester	4
Co-requisites module	None	Semester	

Module Aims, Learning Outcomes and Indicative Contents	
Module Aims أهداف المادة الدراسية	1. Learn about the different digital systems, especially the digital system and the method of arithmetic operations. 2. Understand and understand how a computer performs arithmetic operations and how numbers and letters are represented in digital circuits. 3. Giving bases and concepts about encoding digital and text data inside the computer. 4. Develop the student's ability to design, analyze and implement the work of the synthetic digital circuit according to the equation or truth table. 5. Develop the student's ability to design, analyze and implement the synthetic digital circuit as required by the narrative. 6. Identify the work and analysis of some commonly used circuits in digital systems. 7. Teaching the student how the computer stores digital information and transmits it within the components of the computer. 8. Develop the student's ability to diagnose faults or errors in the work of synthetic digital circuits and repair them.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Training the student to enjoy the designer's mindset in different cases. 2. Making the student able to adapt to different circumstances and solve problems with the least available. 3. Converting the design from paper and pen to digital circuits that work either on the computer or on digital reality. 4. Recognize and understand all the principles of logical design 5. Recognize and understand how to understand and work with computer architecture and other digital systems. 6. The ability to analyze and discover the problem or error and the ability to find a solution to the error. 7. Develop the student's mentality to be able to make the theoretical requirement identical to the circuit he designs. 8. Develop students' skills in employing mathematical theories and equations to solve applied problems. 9. The ability to design and analyze multiple digital circuits using computer languages or virtually.

	10. The ability of the student to build and form more complex digital circuits by connecting smaller digital circuits. 11. The ability to test all designed digital circuits and the ability to detect errors, if any.
Indicative Contents المحتويات الإرشادية	Indicative content includes the following. Part A – Digital Fundamental and Combinational Logic Design Number Systems, Operations, and Codes, Logic Gates, Boolean Algebra and Logic Simplification, The Karnaugh Map, Combinational Logic Analysis, The Universal Property of NAND and NOR gates, Pulse Waveform Operation, Functions of Combinational Logic. [15 hrs] Revision problem classes [6 hrs] Part B – Sequential Circuits Latches, Flip-Flops, Timers, Flip-Flop Operating Characteristics, Flip-Flop Applications, One-Shots, The Astable Multivibrator, Shift Register Operations, Finite State Machines, Asynchronous and Synchronous counters, Cascaded Counters, and Logic Symbols with Dependency Notation.[15 hrs] Revision problem classes [6 hrs] Part C: Programmable Logic and Data Storage [15 hrs] Revision problem classes [6 hrs] Part D: Signal Conversion and Processing Revision problem classes [6 hrs]

Learning and Teaching Strategies

استراتيجيات التعلم والتعليم

Strategies	1. Giving lectures and solving mathematical problems on the board. 2. Using modern technologies and electronic data show means to clarify the shapes, drawings, diagrams, and lecture vocabulary. 3. Focusing on students' participation in the lecture by asking questions, eliciting new ideas, and finding other ways to solve mathematical problems. 4. Adopting the homework method to solve the exercises by the students, while evaluating their solutions in the classroom.
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Student Workload (SWL)

الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	108	Structured SWL (h/w) الحمل الدراسي المنتظم للطالب أسبوعيا	7
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	67	Unstructured SWL (h/w) الحمل الدراسي غير المنتظم للطالب أسبوعيا	4.5
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	175		

Module Evaluation

تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	10% (10)	5, 10	LO #1, 2, 10 and 11
	Assignments	2	10% (10)	2, 12	LO # 3, 4, 6 and 7
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	LO # 5, 8 and 10
Summative assessment	Midterm Exam	3 hrs.	10% (10)	7	LO # 1-7
	Final Lab Exam	2 hrs	10%(10)	16	All
	Final Exam	3 hrs.	40% (10)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

المنهاج الاسبوعي النظري

	Material Covered
Week 1	Introduction - Number Systems (Binary, HEX, BCD)
Week 2	Number System Arithmetic (Signed and Unsigned) and Digital Codes
Week 3	Logic Gates, Boolean Operations and Expression, Laws and Rules of Boolean, DeMorgan Theorm.
Week 4	Logic Simplification Using Boolean Algebra, SOP & POS, Boolean expression and Truth Tables
Week 5	The Karnaugh Map, (Karnaugh Map SOP Minimization, Karnaugh Map POS Minimization)
Week 6	Implementing of Combinational Logic Circuits (Adders, Parallel Adders, Comparators)
Week 7	Decoders, Encoders, Code C Code Converters, Multiplexers (Data Selectors), Demultiplexers, Parity Generators/Checkers
Week 8	Sequential Logics (Latches, Flip-Flops) and their applications
Week 9	One-Shot Monostable Circuit, Astable Multivibrator, 555 Oscillator
Week 10	Shift Register Operations, Types of Shift Register Data I/Os, Bidirectional Shift Registers Shift Register Applications
Week 11	Asynchronous Counters, Synchronous Counters, Up/Down Synchronous Counters
Week 12	Design of Synchronous Counters, Cascaded Counters
Week 13	Counter Decoding, Counter Applications
Week 14	Programmable Logic Devices (CPLDs, FPGAs)
Week 15	Signal Conversion and Processing (ADC and DAC)
Week 16	The preparatory week before the Final Exam

Delivery Plan (Weekly Lab. Syllabus)

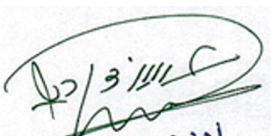
المنهاج الاسبوعي للمختبر

	Material Covered
Week 1	Lab 1: Basic Logic Gates (AND – OR – NAND – NOR – XOR – XNOR)
Week 2	Lab 2: Combinational Logic Circuits 1- Full Adder , Parallel bit Adders, 4-bit binary Full Adder, cascaded Full Adder 2- Comparators, Multiplexers, De-Multiplexer, Parity Generators/Checkers
Week 3	Lab 3: Decoder, Encoders, Cascaded Decoder, Cascaded Encoder
Week 4	Lab 4: Latch circuits, S-R Flip Flop, D-Flip-Flop, J-K Flip Flop, T-Flip Flop
Week 5	Lab 5: One Shot circuits (Monostable, Astable)
Week 6	Lab 6: Counters, Cascaded Counters, Shifts Registers
Week 7	Lab 7: ADC and DAC circuits

Learning and Teaching Resources		
مصادر التعلم والتدريس		
	Text	Available in the Library?
Required Texts	1. Digital Fundamental (Thomas Floyd)	Yes
Recommended Texts	1. Digital Circuits And Logic Design (Samuel C Lee) 2. Digital Logic & Computer Design (Mano) 3. Digital Design: With an Introduction to Verilog HDL	No
Websites	1. http://freecomputerbooks.com/ 2. https://www.tutorialspoint.com/computer_logical_organization/index.htm 3. http://www.electronicengineering.nbcafe.in/ 4. https://www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/	

Grading Scheme				
مخطط الدرجات				
Group	Grade	التقدير	Marks (%)	Definition
Success Group (50 - 100)	A - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	FX – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required
Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.				


Head of the Department
Dr. Osama Abdulbari


أ.م.د. حسين هادي حسين
عميد كلية الهندسة


علي محمد